REMARKS

The Examiner has maintained the same rejections that were made in the previously submitted Office Action dated June 16, 2006. In Section II (REJECTIONS BASED ON PRIOR ART) of the last Office Action dated October 23, 2006, the Examiner has restated the arguments previously stated in Section VI (REJECTIONS BASED ON PRIOR ART) of this Office Action. As a consequence, the Applicants request that the Examiner refer to the arguments previously made in the Response to Office Action dated July 25, 2006. Furthermore, the Applicants have provided the following arguments in response to Section V (ARGUMENTS CONCERNING PRIOR ART REJECTIONS) of the Office Action dated October 23, 2006.

35 USC § 102 REJECTIONS

CLAIMS 1-2, 6, 12-13, and 15-19

The Examiner has rejected Claims 1-2, 6, 12-13, and 15-19 under 35 U.S.C. 102(b) as being anticipated by Hinton et al. (US 5,500,948), hereinafter "Hinton."

Per the Examiner's first Point of Argument, Applicants have noted that the Examiner's position with respect to Claims 12, 16, and 18 is to use the same rationale used in the Examiner's argument for Claim 1. With respect to Examiner's 2nd Point of Argument, the Applicants maintain their stance with respect to the previous argument provided in the Response to Office Action of July 25, 2006. Claim 1 recites "a method of reducing the size of a translation lookaside buffer comprising utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of said translation lookaside buffer". Nowhere does Hinton disclose all the elements and features as recited in Claim 1. For example, Applicants have not found any

teaching or disclosure in Hinton of "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as recited in Claim 1. The Examiner simply refers to Figure 3 and portions of passages found in Column 6, lines 37-63; and Column 7, lines 5-14 of Hinton without providing any evidence and/or logical explanation of how each of the features in Claim 1 are taught by these passages. For example, the Applicants respectfully submit that nowhere do these passages teach "utilizing a bit obtained from a virtual page number of a virtual address for the purposes of writing and reading even and odd page frame numbers into a single page frame number field of a translation lookaside buffer," as recited in Claim 1. For example, Applicants request that the Examiner locate where within Hinton there is any disclosure of a "virtual page number" as recited in Claim 1. Furthermore, for example, Applicants request that the Examiner locate where within Hinton there is any disclosure of "writing and reading even and odd page frame numbers into a single page frame number field" (i.e., as opposed to a writing and reading even and odd page frame numbers into two page frame number fields). Applicants respectfully submit that none of the foregoing features is taught or disclosed in Hinton. Finally, Hinton does not disclose or teach a method of *reducing the size* of a translation lookaside buffer. Hinton is different from the claimed invention since Hinton's invention has nothing to do with reducing the size of a buffer, as recited in Claim 1. Therefore, the Applicants respectfully submit that Claim 1 contains patentable subject matter that should be allowed. Since Claims 2-11 depend on an allowable Claim 1, these claims should be allowed as well. Therefore, for at least the foregoing reasons, Applicants respectfully request allowance of Claims 1-11.

As per the Examiner's 3rd Point of Argument, Applicants respectfully submit that Hinton does not teach utilizing a bit that corresponds to a least significant bit of a *virtual page number*,

as recited in Claim 2 (emphasis denoted in italics). In response to the Examiner's comment in section 12 of the Office Action (that references Column 6, lines 37-63; Figure 3) is that "a logical address (81) is separated into three parts. Bits 0 through 11 are an offset within an instruction page" and explains that "bit 12 selects which of the two entries in the TWB (62) are to be used for this address", the Applicants respectfully submit that Hinton's "bit 12" does *not* teach a least significant bit as recited in Claim 2 of the present Application. As taught by Hinton, "bit 12" is one of three parts in a logical address, of which the logical address comprises 32 bits. Furthermore, nowhere is there any disclosure in Hinton of "a least significant bit of a virtual page number," as recited in Claim 1. As a consequence, for at least this reason alone, Applicants request allowance of Claim 2.

As per Claim 12, the Applicants stand by the arguments made in the previous Response to Office Action of July 25, 2006. Applicants fail to see how Hinton teaches what is recited in Claim 12. For example, nowhere does Hinton teach "a translation lookaside buffer comprising using a bit obtained from a virtual page number to consolidate even and odd page frame numbers into a single page frame number field of said translation lookaside buffer", as recited in Claim 12. Nowhere does Hinton disclose or mention using "a bit obtained from a virtual page number" or "a single page frame number field of a translation lookaside buffer (TLB)." Furthermore, Hinton is different since Hinton discloses a data processing system comprising a translation lookaside buffer (TLB) and an improvement comprising "a logical address bus connected to said TLB and to said TWB, said logical address bus presenting an instruction pointer to the said TLB and to said TWB, said instruction pointer comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, said single bit providing for translation of even-number pages for which said single bit has said first value and

for odd-number pages for which said single bit has said second value" [Column 9, lines 26-30; Column 10, lines 6-16]. Therefore, Hinton's invention uses two buffers (i.e., a TLB and a TWB) compared to Applicants' claimed invention which recites a single buffer (i.e., a TLB). As per Examiner's 4th Point of Argument with respect to Claim 12, Examiner's argument is to simply refer to the same passages that were previously referenced with respect to Claim 1. Again, the Examiner simply refers to Figure 3 and portions of passages found in Column 6, lines 37-63; and Column 7, lines 5-14 of Hinton without providing any logical explanation of how the features recited in Claim 1 are taught by these passages. Therefore, for each of the foregoing reasons, the Applicants respectfully submit that Claim 12 contains patentable subject matter. Since Claims 13-15 are dependent on independent Claim 12, Applicants respectfully submit that these claims are allowable as well.

As per Claim 13, the Applicants stand by the arguments made in the previous Response to Office Action of July 25, 2006. Furthermore, the Applicants request the Examiner to refer to the arguments provided for Claim 2 in the current Response to Office Action. As a consequence, for at least this reason alone, Applicants request allowance of Claim 13.

As per Claims 12, 16, and 18, the Applicants stand by the arguments made in the previous Response to Office Action of July 25, 2006. Furthermore, as per Claims 12, 16, and 18, the Applicants fail to see how Hinton teaches all the features recited in each of these claims. The Applicants request the Examiner to refer to the arguments previously provided for Claim 1. As a consequence of the foregoing arguments, the Applicants request the Examiner to withdraw her rejection to Claims 16, 18, and 18.

Because of the foregoing detailed arguments presented in response to the Examiner's 35 USC 102 rejections, Applicants feel that the pending claims should be allowed.

35 USC § 103 REJECTIONS

CLAIMS 3, 5, 10, 14 and 20

As for Claims 3, 5, 10, 14, and 20, the Applicants stand by the arguments made in the previous Response to Office Action of July 25, 2006. In the Office Action of June 16, 2006, the Examiner had admitted that Hinton does not expressly disclose "wherein said reading and writing is performed by way of using an existing translation lookaside buffer (TLB) control processor instruction set" and "wherein said translation lookaside buffer of reduced size is compatible with one or more legacy systems utilizing any existing TLB instructions, software, or commands". The Examiner had taken official notice that it "would have been obvious to one of ordinary skill in the art at the time the invention was made to use an existing translation lookaside buffer control instruction set and make the translation lookaside buffer as taught by Hinton compatible with existing TLB instructions, software, or commands as one of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system components." Applicants had traversed and/or challenged the Examiner's official notice, and requested that if the Examiner maintains (or wishes to maintain) the rejections for Claims 3, 5, 10, 14, and 20, that the Examiner produces documentary evidence to support her assertion. The Examiner has referenced Column 3, lines 23-25 and Column 3, lines 57-62 of Hinton. Applicants fail to see how the Examiner has established a prima facie case of obviousness by referencing features or elements that are not recited in Claims 3, 5, 10, 14, and 20. As per Examiner's 5th Point of Argument, Applicants do not clearly understand the Examiner's remark that "therefore, any kind of instructions [sic] may be used as any instruction used in Hinton's disclosure is an existing/legacy instruction."

Furthermore, Applicants do not see where the Examiner shows a *suggestion* or *motivation* to combine Hinton and Kirk based on what is *disclosed* by Hinton and/or Kirk. As a consequence, the Applicants respectfully submit that the Examiner has failed to provide a prima facie case of obviousness to reject Claims 3, 5, 10, 14, and 20. With regard to Claim 10, none of the remarks made by the Examiner have addressed the features recited in Claim 10. Furthermore, the Examiner has not shown a motivation or suggestion to combine the cited references, Hinton and Kirk, as cited by the Examiner. Finally, ascertaining the differences between the prior art and the claims at issue requires interpreting the claim language, and considering both the invention and the prior art references as a whole (MPEP at § 2141.02). As a consequence, the Applicants feel that it would not be obvious to combine the references, as cited by the Examiner, because each of the inventions presented by each reference, when taken as a whole, is distinctly different from each other. For at least each of the foregoing reasons, the Applicants request the Examiner to withdraw the rejections to Claims 3, 5, 10, 14, and 20.

Per Examiner's 6th Point of Argument, the Applicants acknowledge the Examiner's withdrawal of the remark that "a recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior if prior art has the capability to do so," in the Office Action of June 16, 2006. As a consequence, the argument posed by the Examiner fails to adequately support rejections to Claims 3, 5, 10, and 14. Therefore, the Applicants request the Examiner to withdraw the rejections to Claims 3, 5, 10, and 14.

CLAIMS 4 and 11

As for Claims 4 and 11, the Applicants stand by the arguments previously made in the Response to Office Action of filed on July 25, 2006. Previously, the Examiner has admitted that

"Hinton does not disclose expressly that said TLB control processor instruction set comprises a MIPS control processor instruction set." The Applicants had traversed the official notice associated with the Examiner's remark that: "It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an instruction set which comprises a MIPS (Millions Instructions Per Second) {sic} processor instruction set which is a well-known processor type. One of ordinary skill in the art would have been motivated to select from off the shelf processors at least to reduce cost and take advantage of existing system component designs." The Applicants respectfully submitted that the Examiner's characterization of what is recited in Claims 4 and 11 was incorrect and that MIPS referred to a RISC microprocessor architecture developed by MIPS Technologies (aka MIPS Computer Systems Inc.). As per Examiner's 7th Point of Argument, Applicant respectfully submits that the subject matter claimed in Claims 4 and 11 is not well-known when taken in context with the claimed subject matter provided by independent Claim 1 and the intervening claims, which it depends on. For example, nowhere does Hinton teach or disclose a method of *reducing* the size of a translation lookaside buffer comprising utilizing a single bit from a virtual page number, wherein said reading and writing is performed by way of an existing translation lookaside buffer (TLB) control processor instruction set comprising a MIPS control processor instruction set, as recited in dependent Claim 4 and base Claim 1, including intervening Claim 3. Likewise, nowhere does Hinton teach or disclose a method of *reducing* the size of a translation lookaside buffer comprising utilizing a single bit from a virtual page number, wherein said reading and writing is compatible with one or more existing TLB registers, said TLB registers comprising TLB registers defined by a MIPS architecture, as recited in dependent Claim 11 and base Claim 1, including intervening Claim 10. Because of the foregoing reasons, Applicants fail to see how the Examiner has established a

prima facie case of obviousness. As a consequence, the Applicants request that the Examiner allow Claims 4 and 11.

CLAIM 7

As for Claim 7, the Examiner has rejected Claim 7 under 35 U.S.C. 103(a) as being unpatentable over Hinton in view of Bryg et al. (US 6,430,670), hereinafter "Bryg." The Examiner admits that Hinton does not disclose that "said virtual page number is defined by bits [31:12] of said 32 bit virtual address," as recited in Claim 7. Based on Column 4, lines 9-20 of Bryg, the Examiner believes that "positions of a virtual page number bits [sic] vary depending on the page size used in the virtual mapping and are system-specific as taught by Bryg." Further, the Examiner has stated that the "Applicant [sic] has [sic] not disclosed that defining a virtual page number within specific bit positions of a virtual address provides an advantage, is used for a specific purpose, or solves a stated problem." It is unclear to the Applicants as to exactly what the Examiner means by the preceding statement. However, as may be referenced in 35 USC 101, "whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, ..." As a consequence, the Applicants respectfully submit that what is recited in dependent Claim 7 (which depends on base Claim 1) provides a new and useful process of "reducing the size of a translation lookaside buffer." Furthermore, Applicants respectfully submit that the subject matter claimed in Claim 7 is not well-known when taken in context with the limitations provided by independent Claim 1, which it depends on. For example, nowhere do the references (Hinton and Bryg), in combination, teach or disclose a method of *reducing* the size of a translation lookaside buffer comprising utilizing a single bit from a virtual page number, wherein

the virtual page number is defined by bits [31:12], as recited in dependent Claim 7 (emphasis denoted in italics). Furthermore, the Applicants submit that *the Examiner* has provided the motivation to combine Hinton and Bryg; however, the *references themselves* have not taught or suggested a desirability to combine as required for a prima facie case of obviousness (emphasis denoted in italics). As a consequence of each of the foregoing reasons, Applicants request withdrawal of the obviousness rejection and allowance of Claim 7.

CLAIMS 8-9

With respect to the Examiner's 8th Point of Argument, the Examiner has rejected Claims 8-9 under 35 USC 103(a) as being unpatentable over Hinton in view of Riedlinger et al. (US 6,446,187), hereinafter "Riedlinger." The Examiner references Column 4, lines 14-23 of Riedlinger. However, nowhere does Riedlinger disclose a "page mask size ranging from 4 kilobytes to 16 megabytes" as recited in Claim 8. Applicants disagree with the Examiner's statement that the "Applicant (sic) has not disclosed that [having a virtual address utilize a page mask ranging from 4 kilobytes to 16 megabytes or a page mask of 4 kilobytes] provides an advantage, is used for a particular purpose, or solves a stated problem." Furthermore, the Applicants request that the Examiner provide evidence in the MPEP that requires the Applicants to disclose that claimed subject matter must provide an advantage, is used for a particular purpose, or solves a stated problem. As the Applicants understand, 35 USC 101 states that "whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, ..." Applicants submit that "reducing the size of a translation lookaside buffer," as recited in base Claim 1 comprises a new and useful process. Furthermore, Applicants

respectfully submit that the subject matter claimed in Claims 8-9 is not well-known when taken in context with the claimed subject matter provided by independent Claim 1 and the intervening claims, which it depends on. The Applicants respectfully submit that the page mask size as used in the various aspects of Applicants' claimed invention provides a preferred embodiment (i.e., a preferred range) in which the claimed invention may be realized. Finally, the Applicants submit that *the Examiner* has provided the motivation to combine Hinton and Riedlinger instead of using what is provided by the references themselves, as evidenced in her remark that "it is the Examiner's position that the [sic] since the size of a page of a TLB is variable and a matter of design choice, the page mask used to select a virtual page size may also vary depending on the size of the TLB used and it is also a matter of design choice." The *references themselves* have not taught or suggested a motivation to combine as required in a prima facie case of obviousness (emphasis denoted in italics). As a consequence, Applicants request that the Examiner withdraw the obviousness rejections of Claims 8-9. For at least each of the several foregoing reasons alone, the Applicants request withdrawal of the obviousness rejections and allowance of Claims 8-9.

Application No. 10/750,523
In Response to Office Action Mailed on October 23, 2006
Response Dated: December 15, 2006

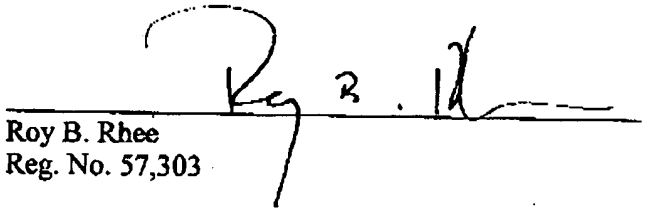
CONCLUSION

Based on at least the foregoing, the Applicants believe that Claims 1-20 are in condition for allowance. A Notice of Allowance is courteously solicited. Should the Examiner disagree, the Applicants kindly request the Examiner to telephone the undersigned at (312) 775-8246.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: December 15, 2006

Respectfully submitted,



Roy B. Rhee
Reg. No. 57,303

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661-2565
Telephone: (312) 775-8246
Facsimile: (312) 775-8100